N-Channel 2.5-V (G-S) Battery Switch, ESD Protection

CHARACTERISTICS

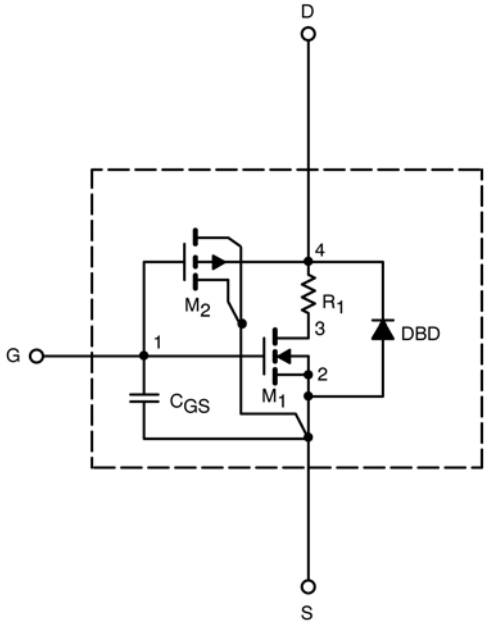
- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the −55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the −55 to 125°C temperature ranges under the pulsed 0-V to 5-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC

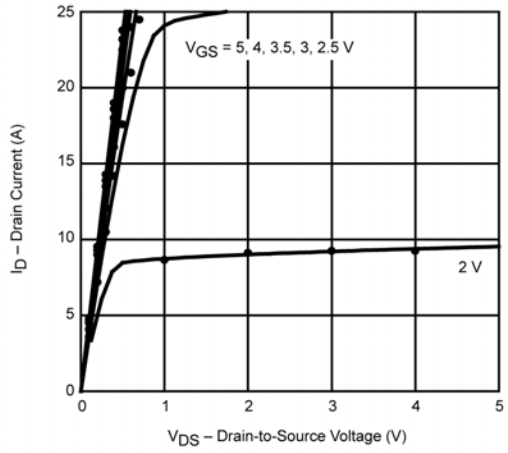


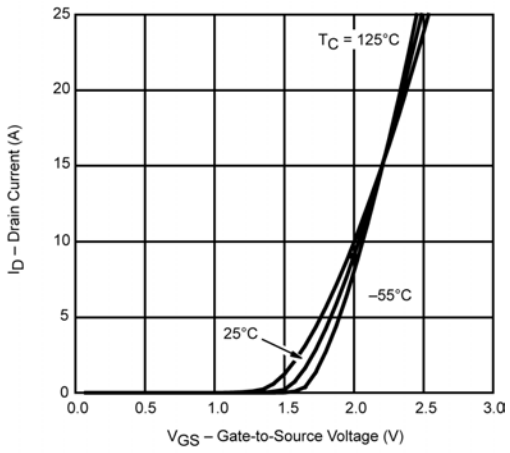
This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

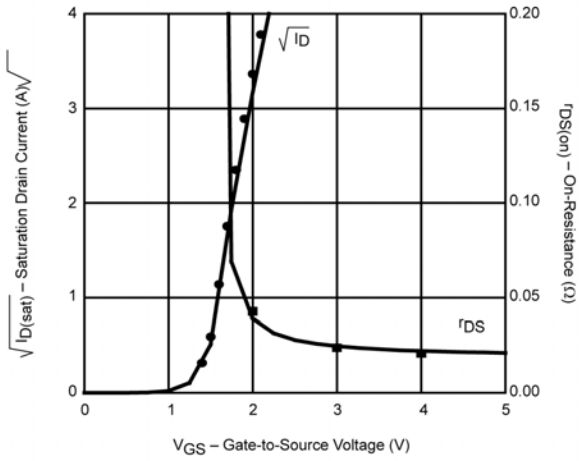
SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)					
Parameter	**Symbol**	**Test Condition**	**Simulated Data**	**Measured Data**	**Unit**
Static					
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	1		V
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} = 5 V, V_{GS} = 4.5 V	128		A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = 4.5 V, I_D = 4.6 A	0.022	0.022	Ω
		V_{GS} = 3 V, I_D = 4.3 A	0.024	0.025	
		V_{GS} = 2.5 V, I_D = 4.1 A	0.027	0.029	
Forward Transconductance[a]	g_{fs}	V_{DS} = 10 V, I_D = 4.6 A	29	25	S
Dynamic[b]					
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 10 V, R_L = 10 Ω I_D ≅ 1 A, V_{GEN} = 4.5 V, R_G = 6 Ω	1.4	0.95	μs
Rise Time	t_r		2.5	1.4	
Turn-Off Delay Time	$t_{d(off)}$		5	7	
Fall Time	t_f		3.3	1.3	

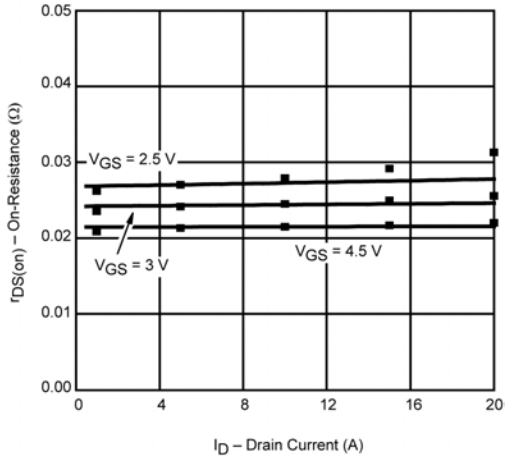
Notes
a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

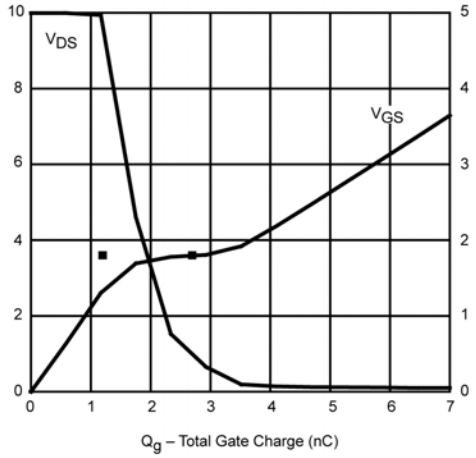
COMPARISON OF MODEL WITH MEASURED DATA (T_J=25°C UNLESS OTHERWISE NOTED)











Note: Dots and squares represent measured data.

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